#8/A 2816

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE 8/8/02

In re application of

Katsuji KIMURA

Appln. No.: 09/940,472 Group Art Unit: 2816

Confirmation No.: 4891 Examiner: Minh T. NGUYEN

Filed: August 29, 2001

For: LINEAR VOLTAGE SUBTRACTOR/ADDER CIRCUIT AND MOS DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated May 9, 2002, please amend the above-identified application as follows:

IN THE ABSTRACT:

A voltage subtractor/adder circuit has a differential pair having first and second MOS transistors. Gate electrodes of the first and second MOS transistors form input terminals for receiving an input differential voltage. Drain electrodes of the first and second MOS transistors form output terminals for outputting a subtraction output signal. Source electrodes of the first and second MOS transistors are commonly coupled to form an output terminal for addition output voltage. The sum of currents flowing through the first and second MOS transistors